Session E: Instrumentation and Technologies for Interplanetary Missions

Development of a Ruggedized Rubidium CPT Clock Platform



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



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Presentation Overview

- Background and motivation
- Concept
- Preliminary test results
 - Power consumption
 - Short-term stability / phase noise
- Prototype test results
 - Radiation testing
- Summary



Coherent Population Trapping (CPT) Background

- <u>Technology</u>: Coherent Population Trapping (CPT) architecture enables simplification / power reduction of physics package
- <u>Key features</u>: Low SWaP, with atomic clock accuracy and precision
- <u>History</u>: First demonstrated in 1978. 1990s VCSEL technology provided a path toward commercialization
- <u>Development</u>: Initiated in 2001 with Draper and Sandia Laboratories (DARPA contract) to create a CSAC
- <u>Improved</u>: manufacturability 2009 to 2013 (Army / ManTech Contract)







Replaces lamp with VCSEL, uW directly applied to VCSEL, low SWaP



3 Requires resonant uW cavity, RF discharge lamp (1W), multiple cells , ovens, controllers

Motivation

Shorter / more frequent / low-cost missions in LEO*

→ Require COTS availability with radiation tolerance and a desire for latest technology

- Defense / Commercial applications
 - ✓ LEO space defense
 - Optical time transfer
 - ✓ Inter-satellite communications
 - ✓ Earth observation
 - ✓ Ionosphere weather monitoring
 - ✓ Radio Frequency (RF) geolocation
 - ✓ Interferometry
 - ✓ Tactical MILSATs

Some missions require higher stability than Space CSAC \rightarrow Space MAC (Rb) desired

Space CSAC Heritage

- > 740 units shipped since 2018
- > 40 unique clients
 - Multiple NASA Science missions (CAPSTONE cislunar, CHOMPTT)





Architecture

Simple Block Diagram

Assembly





New Architecture



Limitation: upper operating temperature predicated by cell temperature **Solution: use TEC to help maintain cell temperature**



Ruggedization and Improvement Goals

Ruggedization

- Increased temperature range
 - -40 to > +85 °C
- Packaging
 - Hermetic
 - Vented space variant
 - Rugged I/O (D-sub, SMA)
 - Height < 0.7 in.



Performance and Features

- Features
 - Low Noise
 - ADEV (1S) < 2E-12 [Goal]
 - Phase Noise (1Hz) < -100 dBc/Hz [Goal]
 - Radiation-tolerant option
 - >30 Krad [Goal]
- Maintain key features
 - 1 PPS disciplining
 - Robust telemetry diagnostics
- Maintain (or improve) key stability metrics
 - TempCo < 5E-11
 - ADEV floor ~ ppE-13
 - Aging < 5E-11 /month (freq. drift rate)



Ruggedized Rb Model 8300C LN

Experimental Results



Low-Noise Configuration 8300C LN

Goals

- 1. Improve ADEV < 100s
- 2. Improve Phase Noise
- 3. Minimize added power

EMXO "Deadbugged" into ' assembly





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Projected <6W at maximum operating temperature



Combined Power Draw of 8300C, TEC and EMXO

Projected <6W at maximum operating temperature

	Goal	TOTAL (calculated)	EMXO (typical)	TEC + 8300b (calculated)	
Warm-up power (W)	20	15.5	1.5	14	
Power @ -40°C (W)*	16	10.3	0.3	10	
Power @ 25°C (W)	12	6.8	0.3	6.5	
Power @ 65°C (W)		4.8	0.3	4.5	
Power @ 75°C (W)		<5.1	0.3	<4.8	
Power @ 80°C (W)		<5.3	0.3	<5	
Power @ 85°C (W)	8	<5.8	0.3	<5.5	
Power @ 90°C (W)		<6.6	0.3	<6.3	

*temperature measured at

the baseplate

Conclusion: High temperature and LN operation is attainable, without breaching power goal



ADEV of 8300 LN Option



Conclusion: ADEV < 30s is improved with EMXO (blue trace)



Phase Noise of 8300 LN Option

Phase Noise £(f) in dBc/Hz



MICROCHIP

Conclusion: Phase Noise is improved with EMXO (blue trace)

EMXO Optimization

- Effort is underway to optimize the EMXO control circuit and later embed into the 8300C
- Preliminary results are shown next



EMXO breadboard



Predicted ADEV of 8300C LN Option*

***Optimized EMXO**

Allan Deviation $\sigma_v(\tau)$



Conclusion: potential improvement for σ_v (1s) < 6E-13



Predicted Phase Noise of 8300C LN Option*

***Optimized EMXO**

Phase Noise £(f) in dBc/Hz



Conclusion: potential improvement to phase noise



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Ruggedized Rb Model 8300C

Radiation Testing



Radiation Testing

- Performed at UMASS-Lowell
 "Gamma Cave"
- Calibration: initial 10-minute dosimetry exposure was performed on an empty box to verify the dose rate
- DUT was exposed in two phases
 - 1. To 20 Krad
 - Power-cycle and health check
 - 2. Until failure
 - Power-cycle and failure analysis
- Goal: achieve > 30 Krad



Dosimetry orientation with empty box. Dosimeters are attached on the back. (Rear Pb/Al shield not shown in picture.)

8300C samples positioned within the Pb/Al shields.

Performance During 1st Exposure: To 20 Krad

• Frequency output \rightarrow

• Telemetry:

Performance During 2nd Exposure: Until Failure

• Frequency output \rightarrow

• Telemetry:

Total Radiation Dosage - TID = 36.1 Krad

Space MAC-8300C and EMXO Test Results

- Space MAC-8300C prototype survived 36.1 Krad TID (Si)
- <u>Post-mortem diagnosis</u>: Initial analysis points to failures of the ADC and FPGA as a result of radiation exposure
- EMXO breadboard survived > 37 Krad TID
 - Test stopped due to time constraints
- Breadboard still functional post radiation

Summary Table

	MAC-8300C LN			
Technology	CPT Rb clock			
Key Metrics				
Power	7W			
L x W x H	3.25 x 2.75 x 0.69"			
Temperature Range	-40 to +85 °C			
<u>Performance</u>	Goals			
ADEV at 1s	2 x 10 ⁻¹²			
ADEV at 1,000s	6 x 10 ⁻¹³			
Freq Drift (Aging)	1.7 x 10 ⁻¹² /day			
ТетрСо	5 x 10 ⁻¹¹ (max)			
Phase Noise at 1 Hz	-100 dBc/Hz			
Measured Radiation tolerand	<u>ce</u> Prototype			
TID	36.1 Krad			

Planned Availability: Spring 2026

Conclusions and Next Steps

• Experimental Results proved design feasibility toward a wide temperature and low-noise Rb

Next steps

- 1. Integration into ruggedized package ✓
- 2. Optimization and integration of EMXO
- 3. Optimization of TEC set points
- 4. Environmental testing (hermeticity, shock, vibration, radiation, TempCo, TVAC)
- Verify performance on prototype design

Thank You

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