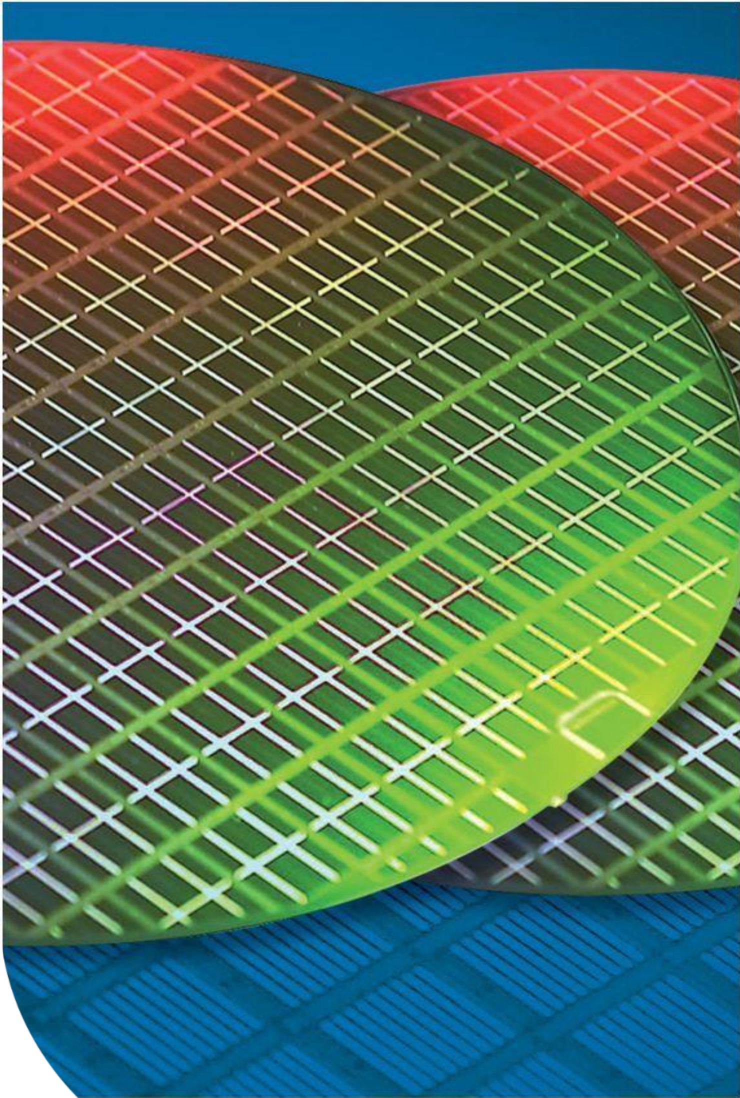
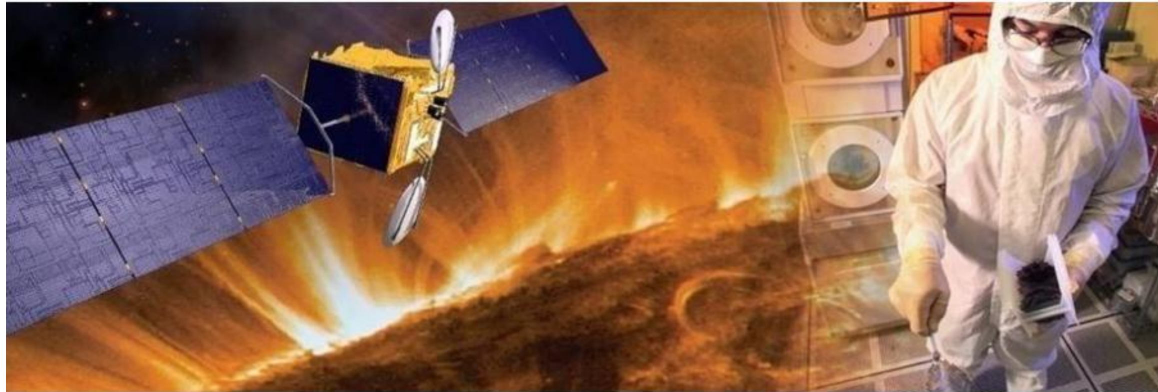
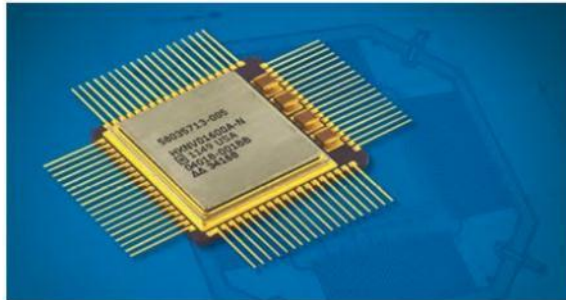
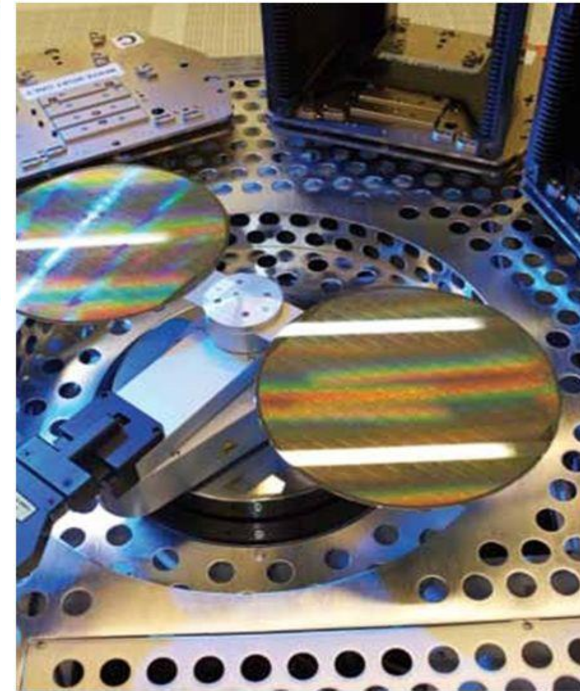
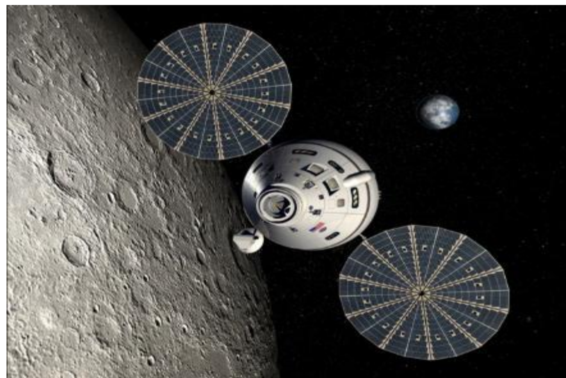

Romney R. Katti, Ph.D.
Presenter

May 12, 2020

HEAVY-ION AND RADIATION-HARDNESS IN MAGNETO-RESISTIVE RANDOM ACCESS MEMORIES (MRAMS)

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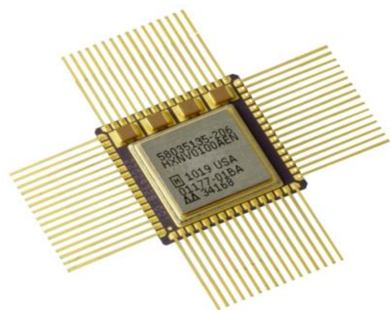
Presentation Overview

- Magnetic Tunnel Junctions (MTJs): Robust Magnetic Bits in MRAMs
  - Reliable spintronic devices: Use electron spin is the fundamental state variable
  - Applications: Magnetic bits in MRAMs as robust Non-Volatile Memories (NVMs)
- Honeywell's Radiation-Hardened Magneto-Resistive Random Access Memories (MRAMs)
  - 1Mb Single Chip Package (SCP) MRAM
  - 16Mb SCP MRAM, QML V, Q qualified, SMD 5962-13212
  - 64Mb Multi-Chip Module (MCM) MRAM, QML V, Q qualified, SMD 5962-14230



Honeywell's
1Mb MRAM

Honeywell's
16Mb MRAM

Honeywell's
64Mb MRAM MCM

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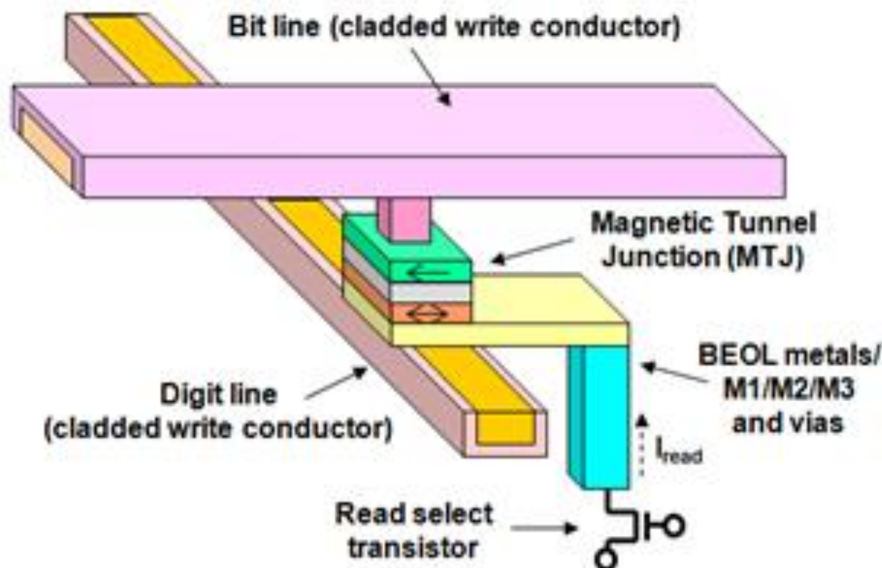
Applying Reliable MTJs: Honeywell's MRAMs

- Non-Volatile Memory (NVM): Magneto-resistive Random Access Memory (MRAM)
- Honeywell’s 16Mb MRAM Single-Chip Package: QML V, Q qualified, SMD 5962-13212
- Honeywell’s 64Mb MRAM Multi-Chip Module: QML V, Q qualified, SMD 5962-14230
  - Read process is based on Tunneling Magneto-Resistance (See the 2007 Nobel Prize in Physics)
  - Write process is based on inductive Savtchenko toggle switching
  - Non-volatile: Data state is retained magnetically including with power off
  - High write endurance, read endurance, and data retention
  - Magnetic Tunnel Junction (MTJ) toggle bits integrated with radiation-hardened S150 CMOS
  - Reliability achieved across fifteen-year specified life with radiation hardness
  - MRAM MTJ Technology is scalable



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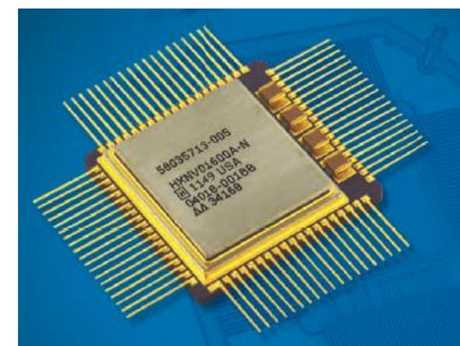
HXNV01600

16 Megabit Non-Volatile Magneto-Resistive RAM



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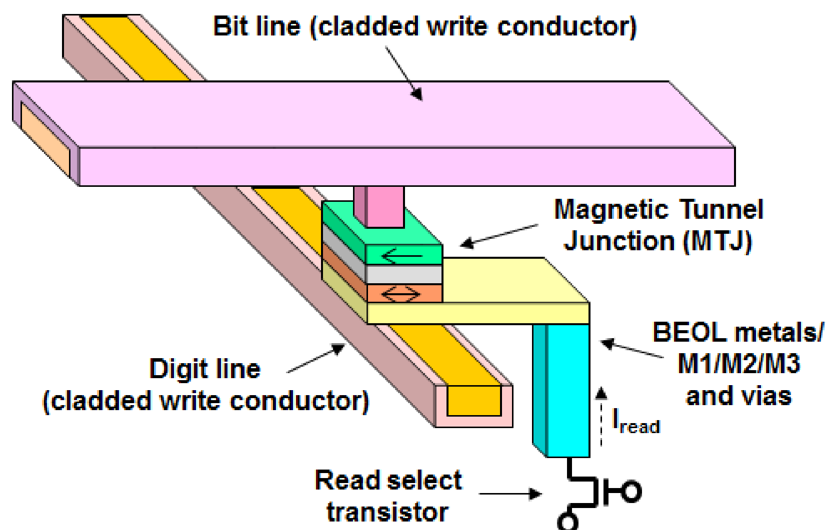
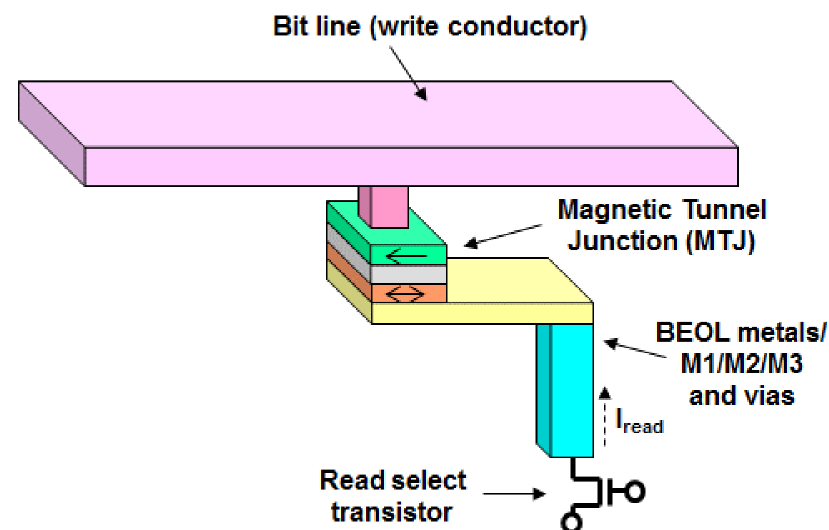
Magnetic Tunnel Junction (MTJ) Memory Bits

- First-generation technology in production
- Megabits regime
- Uses Magnetic Tunnel Junction (MTJ) bits
  - Read: Tunneling Magneto-Resistance (TMR)
  - Write: Inductive Savtchenko switching
- Inductively written toggle bits
  - Read path is through the MTJ
  - Write path is not through the MTJ
  - Voltage to the Tunnel Barrier (TB) is applied only during reading, requiring managing only the read distributions within TB breakdown voltage limits
- Practically unlimited read and write endurance and data retention



- Emerging next-generation technology
- Megabits to Gigabits regime
- Uses MTJ bits
  - Read: TMR
  - Write: Spin-Torque-Transfer (STT) Direct Writing
- Direct writing using electronic spin currents
  - Read path is through the MTJ
  - Write path is also through the MTJ
  - Voltage to the TB is applied during reading and writing, requiring managing both read and write distributions within TB breakdown voltage limits
- Potentially unlimited read and write endurance and data retention



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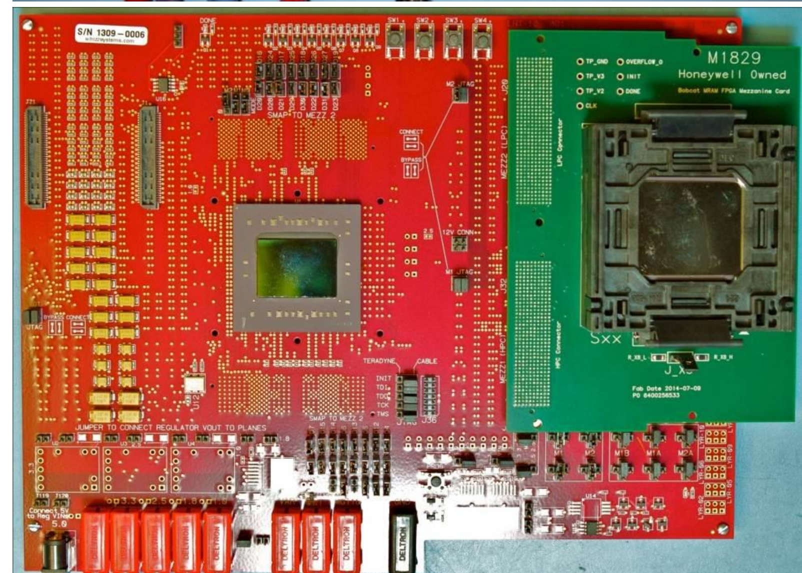
Honeywell MRAM and V5QV FPGA Compatibility

- Demonstrated successful configuration boot of the V5QV FPGA for four 16Mb MRAMs and for the 64Mb MRAM MCM
- Setup Details
  - Red Board: XRTC CPU board
  - Green Board: Honeywell daughter board, with
    - Four 16Mb MRAM packaged parts (top photograph)
    - One 64Mb MRAM MCM (bottom photograph)
- Configuration Details
  - Master SelectMap Mode
  - Auto-detection of x8 and x16 wide bus
  - Confirmed both 2.5V and 3.3V I/O operation



Special thanks to Gary Swift, David Lee, and Mike Wirthlin for their technical support in this configuration demonstration

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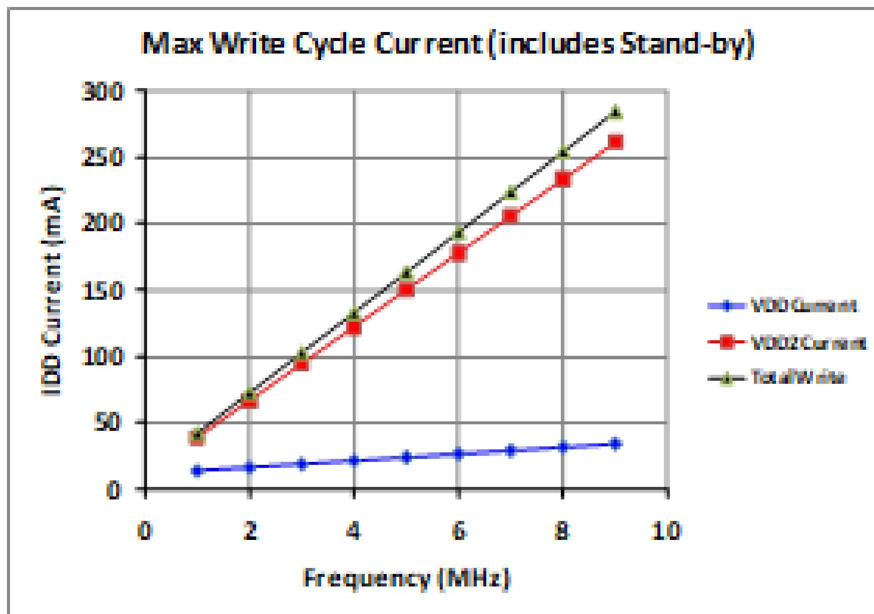
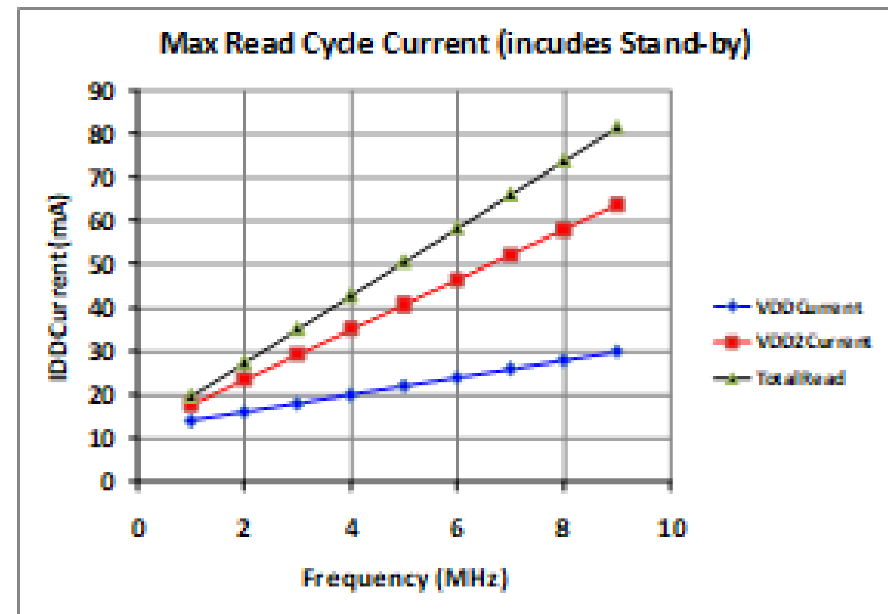
Honeywell's MRAMs are compatible with V5QV FPGAs

Stability and Reliability of Writing and Readback

- Reliability and stability to Total Ionizing Dose (TID) exposure of MTJs and radiation-hardened 150nm CMOS transistors and circuitry
- Write and read currents show linearity, reliability, stability, and linearity with frequency

Parameter metric	Values Normalized to Pre-Irradiation Values, %				
Radiation level	50 krad	100 krad	300 krad	500 krad	1000 krad
Read reference voltage (Co60)	100.1	100.2	100.4	100.5	100.7
Write reference current (Co60)	100.3	100.5	101.0	101.2	101.9
Read cycle time (Co60)	100.0	100.0	100.0	100.0	100.0
Write cycle time (Co60)	100.0	100.0	100.0	100.0	100.0
Pattern test counts (Co60)	100.0	100.0	100.0	100.0	100.0
Read reference voltage (Aracor)	100.1	100.2	100.3	No data	100.6
Write reference current (Aracor)	99.8	99.9	99.9	No data	100.0
Read cycle time (Aracor)	100.0	99.8	99.6	No data	99.3





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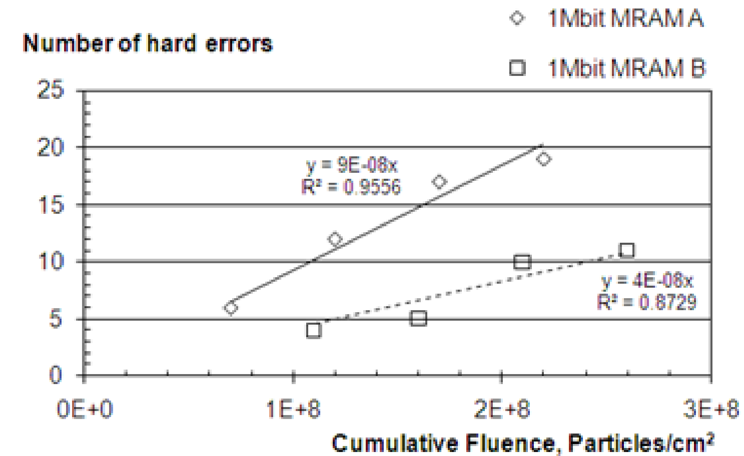
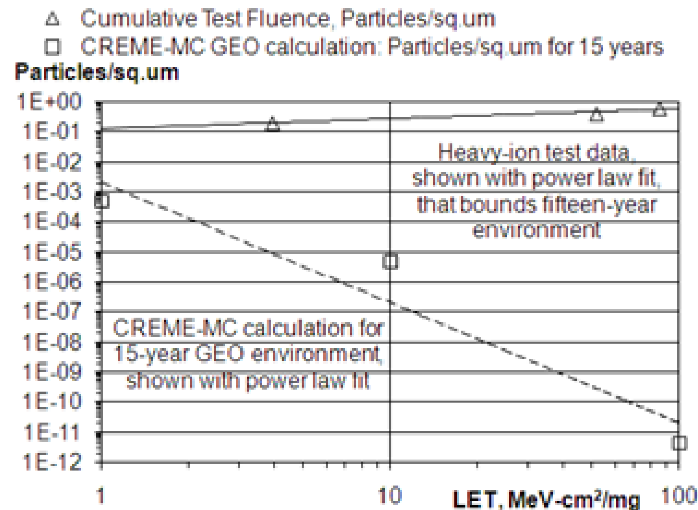
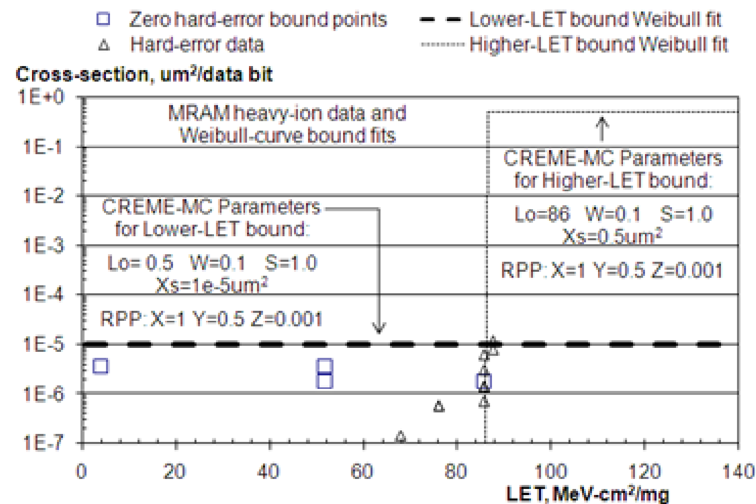
Heavy Ion Single Event Effects Hard-Error Testing

- Heavy-ion testing quantified the rate for inducing hard errors, which conservatively bound heavy ion fluences seen in space environments
- Analysis, which is conservative by orders of magnitude and applies binomial statistics, projects hard-error error-rate performance to be much less than 3.11E-17 word errors per word-day, or much less than 0.074 word errors in one million MRAMs in 100 years under continuous use



Estimated Parameter	Calculation	Result
Data bit hard errors per bit-day w/ ECC off (P_{dbhe})	From CREME-MC simulation	3.85×10^{-10}
Probability of a word error per word-day w/ ECC on	$21!/(19!2!) \times P_{dbhe}^2 = 210 \times P_{dbhe}^2$	3.11×10^{-17}





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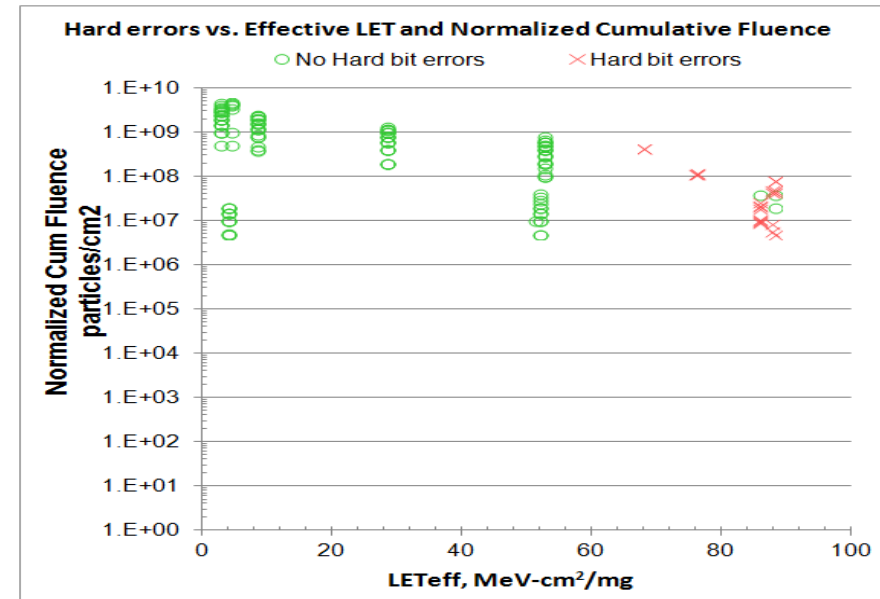
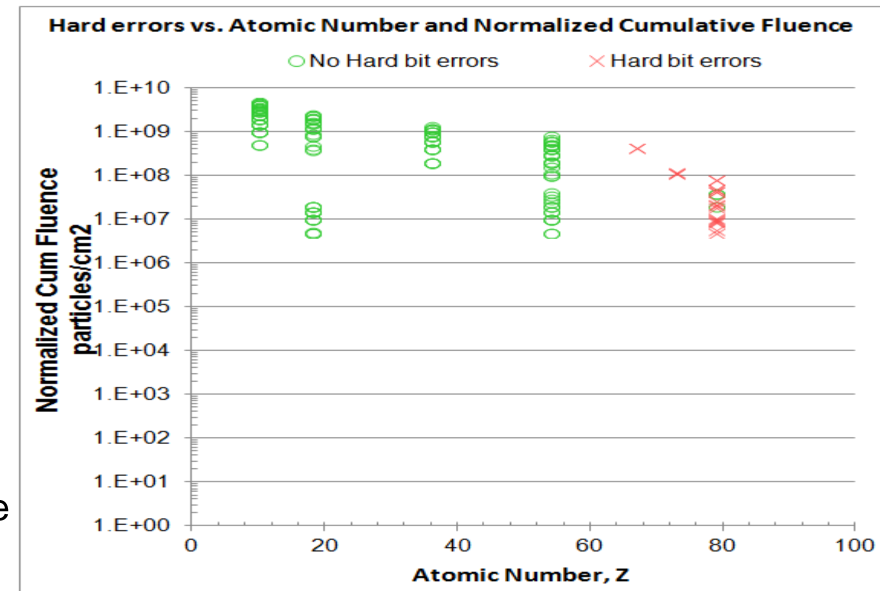
Heavy Ion Single Event Effects Static Testing

- No soft single events observed in static testing
  - Static testing was performed both powered up and powered down with bits in both high and low states
  - No damage of the memory cell bits for Z ≤ Xe or output latch upsets occurred
  - Low level of heavy-ion-induced damage was observed in bits for atomic number > Xe
  - Bit damage occurred irrespective of whether the part was powered up or powered down
- Inducing bit damage requires high LET or high Atomic Number
  - LET >52 MeV-cm^2 /mg or
  - Atomic Number > 54
- Heavy-ion induced bit damage has a low probability of occurring in 15 year life in space
- CREME96 analysis was performed using atomic number Z > 54 and LET > 52MeV-cm^2/mg
- Damaged bit accumulation rate is 1.3E-13 hard errors per bit-day
  - Geosynchronous orbit, solar min non-flare conditions, 100 mil Aluminum shield
  - At 1.3E-13 hard errors per bit-day, in 15 years there could be 1.34E-2 damaged bits per 16Mb MRAM





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MRAM Group E Radiation Qualification

Specification Parameter	Specification Value	Test Performed
Total Ionizing Dose	1 Mrad(Si)	X-ray and Co60 Testing
Single Event Upset	< 1E-10 upsets/bit-day [1]	Heavy Ion Testing TAMU [2]
Dose Rate Upset	16Mb MRAM: 1E10 Rad(Si)/s 64Mb MRAM MCM: 1E09 Rad(Si)/s	Clearwater FXR [3]
Dose Rate Survivability	1E12 Rad(Si)/s	LMTF [4]
Neutron Displacement Damage	1E14 (1 MeV eq.) N/cm^2	S150 Technology + MRAM Bit Testing
Latch-Up	Immune	S150 SOI Immune [5]
Proton Induced Upset	< 1E-10 upsets/bit-day [6]	MRAM Testing + HX5000 Register Data; Confirmed on the 16Mb MRAM by customer testing

[1] Geosynchronous Orbit, Solar Minimum, 100mils aluminum shielding
[2] Texas A&M University
[3] Honeywell Clearwater, Florida, Flash X-Ray Facility
[4] Little Mountain Test Facility at Hill Air Force Base
[5] No latch-up observed during Heavy Ion or DRU Testing
[6] Geosynchronous Orbit, Solar Minimum, 100mils aluminum shielding

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Honeywell's MRAM Passes Qualification Tests

- Passed Group A, B, C, D, and E qualification testing following standards in accordance with MIL-PRF-38535 and MIL-STD-883
  - Passed Group A electrical testing
    - Group A electrical testing includes static, dynamic, and functional testing
  - Passed Group B and Group D package qualification testing
    - Group B Subgroup tests are listed in the next charts
    - Group D Subgroup tests are listed in the next charts
  - Passed Group C (1005) life testing
    - Includes 1000-hour and 4000-hour life tests
    - Demonstrated FIT rate is 24.1 (failures in time, per billion hours of operation), based on zero fails that is limited by accumulated device-hours
  - Passed Group E radiation testing (see the next charts for further details)
    - Performed TID, DRU, DRS, SEE, Neutron, and Proton testing as shown in the next charts
    - SEE was performed dynamically and statically
    - No SEFIs (single-event functional interrupts) were observed, demonstrating SEFI immunity
    - Latch-up immunity is established through the use of SOI CMOS
  - Passed ESD testing
    - Passed HBM (Human Body Model) Class 2 testing (to ±2000 V to ±4000V)
    - Passed MM (Machine Model) Class 4 testing (to >400V to <-400V)
    - Passed CDM (Charge Device Model) Class 5 testing (to ±1000V to ±1500V)
  - Passed stray magnetic field immunity testing
    - Passed 100 Oe in read, standby, and non-operating modes
    - Passed 65 Oe in write mode

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Honeywell's MRAMs pass MIL-STD testing for QML

Honeywell 16Mb and 64Mb MRAM Product Specifications

- Key advantages for Non-Volatile Memory Applications
  - Operation up to 125 °C
  - High write endurance, read endurance, and data retention performance
  - Designed from the ground up for radiation hardness and reliability
  - TID (Total Ionizing Dose) hardness assurance
  - No SEFI sensitivity

Characteristic	Honeywell 16Mb MRAM	Honeywell 64Mb MRAM
SMD Number	5962-13212	5962-14230
QML qualified	V,Q	V,Q
Package	Single-chip package: SCP	Multi-Chip Module: MCM
Package Style	Ceramic Quad Flat Pack	Ceramic Dual Flat Pack
Number of 16Mb MRAM die	1	4
Package leads	76	112
External magnetic shields	Yes	Yes
Power supply voltages	3.3 ± 0.3V (2.5 ± 0.25V I/O option)	3.3 ± 0.3V (2.5 ± 0.25V I/O option)
Address configurations	1M x 16 bits, or 2M x 8 bits	4M x 16 bits, or 8M x 8 bits
Operating Temperature	-40 °C to 125 °C	-40 °C to 125 °C
Read access time, ns	95	100
Read cycle time, ns	120	130
Write cycle time, ns	140	150
Data retention	> 15 years	> 15 years
Endurance	> 1E15 cycles	> 1E15 cycles
TID	> 1 Mrad(Si)	> 1 Mrad(Si)
DRU (transient/operate through)	> 1E10 rad(Si)/s	> 1E9 rad(Si)/s
DRS	> 1E12 rad(Si)/s	> 1E12 rad(Si)/s
Neutron (1 MeV equivalent)	> 1E14 MeV-eq N/cm²	> 1E14 1MeV-eq N/cm²
SEU (radiation)	<1E-10 upsets/bit-day	<1E-10 upsets/bit-day
SEFI (single-event fault interrupt)	None	None
Latch-up	None (SOI immune)	None (SOI immune)
Stray magnetic field immunity	100 Oe non-write, 65 Oe write	100 Oe non-write, 65 Oe write
Error-correction	7-bit Hamming code, single-bit error detection and correction	7-bit Hamming code, single-bit error detection and correction
Addressing features	Auto increment mode for reading sequentially through the address space without an external address	Directly compatible with the Master SelectMap interface on the Xilinx Virtex 5QV FPGA

Honeywell 16Mb MRAM
SMD: 5962-13212
QML V, Q

Honeywell 64Mb MRAM
SMD: 5962-14230
QML V, Q

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Honeywell Memory Roadmap

2013	2014	2015	2016	2017	2018	2019	2020+

SRAM

Legend:

- **Completed Product/Capability**
- **In development**
- **Potential Development**

4Mb SRAM
SMD 5962-08215
16Mb SRAM
SMD 5962-08203

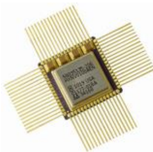
64Mb SRAM
Multi-Chip Module (MCM)
SMD: 5962-10232

18Mb/36Mb SRAM

72Mb/144Mb SRAM MCM

MRAM / Non-Volatile Memory

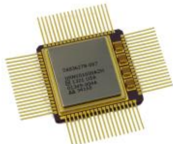
1Mb MRAM



16Mb MRAM
3.3V I/O, QML V,Q
SMD: 5962-13212

16Mb MRAM, 2.5V I/O

≥64Mb MRAM Development



64Mb MRAM (MCM)
SMD: 5962-14230: QML V,Q

Reduced-size 64Mb MRAM MCM
≥64Mb MRAM MCMs

Heterogeneous Integration Development

ASIC-with-MRAM Solutions
≥128Mb Non-Volatile Memory

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Summary

- Magnetic Tunnel Junctions (MTJ) are reliable Spintronic devices that have been successfully integrated with CMOS to create reliable, robust, and radiation-hardened non-volatile Magneto-Resistive Random Access Memories (MRAMs)
- Honeywell's 1Mb MRAM is the first rad-hard non-volatile memory in high volume production offering excellent data retention and endurance
- Honeywell's 16Mb MRAM and 64Mb MRAM MCM are in production and available as QML Q,V standard products
  - Validated MIL-PRF-38535 TCI Group A, B, C, D, and E performance
  - Fifteen-year operating life across temperature with reliability
  - Honeywell's 16Mb MRAM: SMD 5962-13212
  - Honeywell's 64Mb MRAM: SMD 5962-14230
- Performance, reliability, and qualification results of Honeywell's radiation-hardened MRAMs support robustness and suitability for space applications

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