Expandable Hybrid Computing Platform for SmallSats

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Interplanetary missions have a variety of needs for autonomous processing and control. Proposed future mission concepts expect to have more computational resources at their disposal, while operating in smaller spacecraft with stringent SWAP and cost requirements. The CHREC Space Processor v1 (CSPv1) follows a hybrid design philosophy, which surrounds appropriate commercial parts with space-qualified parts to achieve the performance and energy efficiency of a commercial processor with space-qualified reliability. CSPv1 combines a Xilinx Zynq-7020 (with dual ARM cores and reconfigurable FPGA fabric), DRAM (with SECDED coding), radiation-tolerant flash memory (stores multiple boot image copies and user data) with radiation-hardened components for critical systems supplemented with software mitigation for soft errors, all within a 1U printed circuit board. Details of its design and feature set can be found in prior work. CSPv1 forms the computing core of a number of space experiments demonstrating its versatility as a high performance, conveniently expandable computing platform. This paper discusses the expandability, reliability, and future missions for CSPv1.

Customization and hardware expansion are available for CSPv1 through its dense, high-speed 160-pin backplane connector. CSPv1 supports SPI, JTAG, UART, I2C, CAN and Ethernet. The FPGA fabric and backplane connectivity make it possible to add interfaces such as RS-422, RS-485, high speed point to point links or SpaceWire. CSPv1 can be configured with several commercial and open-source operating systems for usability and real-time capability including Linux, RTEMS, and VxWorks. Board-support packages with drivers and applications are available for both RTEMS and Linux platforms. Ancillary testbed development boards provide key interfaces such as Ethernet, JTAG, UART, SpaceWire, CAN, Camera Link, USB, and spare single-ended and differential signals. Flight versions of CSPv1 support NASA Goddard's reusable flight software framework Core Flight Executive (cFE) along with several key Core Flight System applications.

CSPv1 is available in parts grades from commercial space to EEE-INST-002 Level 2. It is manufactured to NASA 8739 workmanship standards, is available with TID tolerance of 30krad or 100krad and immune to destructive single events. Both the ARM cores and the FPGA fabric are susceptible to SEU which are mitigated with various scrubber configurations (blind, readback, or frame-ECC) and watchdog. Block-level TMR can be used in combination for greater reliability. Missions should still tolerate the occasional unexpected reset when the watchdog trips.

Several missions currently in design are using CSPv1's expansion options. A software-defined radio (SDR) consisting of CSPv1, a 1U modem configured for 70MHz IF with 10MHz bandwidth and S-band RF module will be used to evaluate hardware, waveforms and networking protocols for a cluster of CubeSats. A wideband software-defined transmitter (400–4100MHz) with STRS operating environment to provide hardware abstraction for third party waveform development is also being designed. Several CSPv1 boards are to be featured on an upcoming experiment to demonstrate high-performance computing on a clustered and networked space platform. This mission features configurable point-to-point links with networking protocol as the inter-processor communication. The cFE software bus, modified to include OMG Data Distribution Services to support inter-node, publish-subscribe functionality supports communication between all processors.

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